

REMARKS

Claims 1-82 are pending in the application, with claims 1-5 and 15-18 being independent. Claims 2-5 and 8-11 have been amended to correct minor errors. No new matter has been introduced.

Applicants acknowledge with appreciation the Examiner's allowance of claims 2-46, 48-55, 57-64, 66-73 and 75-82.

Claim 1 and its dependent claims 47, 56, 65 and 74 have been rejected as being anticipated by Kane (U.S. Patent No. 6,229,508). Applicant requests reconsideration and withdrawal of this rejection because Kane does not describe or suggest four TFTs interconnected in the manner recited in claim 1. In particular, though the rejection asserts that the transistor N3 of Kane corresponds to the recited fourth TFT, this cannot be the case. As set forth in claim 1, the gate electrode of the fourth TFT is connected to a source or drain region of the second TFT and to a source or drain region of the third TFT. Thus, claim 1 recites that the gate electrode is connected to the connection between the second and third TFTs (node C in the marked up version of Kane's Fig. 7 that is included in the office action).

By contrast, the gate electrode of transistor N3 of Kane is connected to the connection between the transistors N1 and N4, which the rejection equates to the first and second TFTs recited in claim 1 (node B in the marked up version of Kane's Fig. 7 that is included in the office action). While the rejection asserts that the gate electrode of transistor N3 is connected to both node B and node C, this simply is not the case, as the gate electrode is not connected to node C. Accordingly, for at least this reason, the rejection should be withdrawn.

Applicant submits that all claims are in condition for allowance.

Applicant : Kazutaka INUKAI
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No fees are believed to be due. Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 9/2/05


John F. Hayden
Reg. No. 37,640

Customer No. 26171
Fish & Richardson P.C.
1425 K Street, N.W., 11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

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